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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,158	09/25/2003	William P. Delaney	03-0827	7036

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EXAMINER	
KROFCHECK, MICHAEL C	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,158	DELANEY ET AL.	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-12,16,17 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-12,16,17 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/25/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed on 1/31/2006.

2. The specification, and claims 1, 3-7, 10-12, 16-17, 20 have been amended.

3. Claims 8-9, 13-15, 18-19 have been cancelled.

4. The objections/rejections from the prior correspondence not restated herein have been withdrawn.

Claim Objections

5. Claim 6-7, 10 objected to because of the following informalities:

a. In line 9 of claim 6, "transferring the a first..." should read "transferring a first..."

b. The claims not specifically mentioned are objected to because of their dependency.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1-2, 6-7, 11-12, 16-17 rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto et al., US patent 6477619 and Yoshida US patent 6925511.

10. With respect to claim 1, Fujimoto teaches of a storage system comprising: a first storage element (figs. 1, 7, 8, items 1-1-1 and 5), comprising a plurality of disk drives, each configured for storing data (figs. 1, 7, 8; item 5; column 6, lines 41 – 47); and

a first storage controller (figs. 1, 7, 8, item 1-1-1) communicatively coupled to a host computer system (item 1, 7, 8; item 50) and configured for processing I/O requests received from the host computer system (figs. 1, 7, 8; item 1-1-1; column 6, lines 41 –

47, column 7, 6 – 15; where the channel IF unit within the disk array control unit (first storage controller) interfaces with the host computers, and the channel IF unit controls access to the rest of the control unit),

wherein the first storage controller is adaptable to interface with any number of second storage controllers added to the storage system within a second storage elements (figs. 1; column 6, lines 41 – 55; where interconnections 210 and 220 connect the two disk array control units), and

wherein the first storage controller is further adaptable, when adapted to communicate with any of the second storage controllers (figs. 1, 7, 8, item 1-1-2), to route the I/O requests to a selected second storage controller through a switching fabric (figs. 7, 8; column 8, lines 1 – 17 and 32 –40; where the inter-unit paths 141 and 142 may be designed differently for Input and output or equally for bidirectional information transfer)

Yoshida teaches of wherein the first storage controller is adapted to interface with the selected second storage controller via an optional plug-in card (PIC) (fig. 4, 6; column 12, lines 29-50; where the disk control units can be added or removed from the disk control apparatus (PIC) and the service processor manages the disk control units),

wherein the PIC provides circuits not present on the first storage controller to enable N-way connectivity of the first storage controller with said any number of second storage controllers (fig. 4, 6; column 12, lines 22-50; where the disk control apparatus contains a service processor, and various connection networks to connect the multiple disk control units).

Fujimoto and Yoshida are analogous arts as they are both in the same field of endeavor, controlling storage systems. It would have been obvious to one of ordinary skill in the art having the teachings of Fujimoto and Yoshida at the time of the invention to incorporate the service processor, service processor connection network, and the addition/removal of the disk control units as taught in Yoshida into the disk control apparatus in Fujimoto. Their motivation would have been to simplify processing such as adding/removing or moving logical volumes (Yoshida, column 12, lines 31-34).

11. With respect to claim 2, the combination of Fujimoto and Yoshida teaches of all the limitations of the parent claim as discussed supra. Fujimoto also teaches of wherein the storage system is a RAID storage system (fig. 7; column 7, lines 33 – 34).

12. With respect to claim 6, Fujimoto teaches of a method of processing requests from a host computer system (figs. 1, 7, 8, item 50), comprising: receiving requests from a host system in a first storage controller of a first storage element (fig. 8; column 9, lines 17-19)

wherein the first storage element includes a plurality of storage locations in storage devices coupled to the first storage controller (figs. 1, 7, 8, items 1-1-1 and 5; column 6, lines 41 – 47) and

processing the requests to access physical storage locations within the second storage controller (figs. 7, 8; column 9, lines 17 – 26, and 45 – 54; where the read out request is sent from the host computer to the disk array control unit 1-1-1 (first storage controller). The microprocessor determines the location of the data requested and requests the microprocessor in the disk IF units of the corresponding hard drive to read

out the data. If the data is located on a hard drive associated with the disk array control unit 1-1-2 (second storage controller), then it is accessed by the microprocessor within the disk IF units of the disk array controller 1-1-2 (second storage controller) to read out the requested data).

Yoshida teaches of wherein the first storage controller has an optional plug-in card (PIC) for optionally enabling N-way connectivity between the first storage controller and any number of second storage controllers each associated with a corresponding second storage element (fig. 4, 6; column 12, lines 29-50; where the disk control units can be added or removed from the disk control apparatus (PIC) and the service processor manages the disk control units. When multiple disk control units are attached to the disk control apparatus they are coupled to each other);

The combination of Fujimoto and Yoshida teaches of transferring a first portion of the received requests from the first storage controller to a selected second storage controller through the PIC of the first storage controller (Fujimoto; figs. 7, 8; column 9, lines 17 – 26, and 45 – 54; where the read out request is sent from the host computer to the disk array control unit 1-1-1 (first storage controller). The microprocessor in the channel IF unit of disk control unit 1-1-1 forwards the command to the disk IF unit connected to the hard disk drive where the data is stored. In this case the data is stored in a disk on right connected to disk control unit 1-1-2 (second storage controller). This passes through the network connections contained within the PIC in the combination of Fujimoto and Yoshida); and

13. With respect to claim 7, the combination of Fujimoto and Yoshida teaches of all the limitations of the parent claim as discussed supra. Fujimoto also teaches of processing the first portion of the requests with the second storage controller to access physical storage locations on storage devices within the second storage element (figs. 7, 8; column 9, lines 17 – 26, and 45 – 54; where the read out request is sent from the host computer to the disk array control unit 1-1-1. The microprocessor determines the location of the data requested and requests the microprocessor in the disk IF units of the corresponding hard drive to read out the data. For the part of the data located in a hard drive in the disk array control unit 1-1-2 (first portion of the requests), the microprocessor in the channel IF unit in the disk unit 1-1-1 must transfer that read request over the SM and CM paths (switching fabric) to the disk array control unit 1-1-2. It is then received by the microprocessor within the disk IF units of the disk array controller 1-1-2 associated with the desired hard drive which then reads out the data from the hard drive (processes the request)).

14. With respect to claim 11, Fujimoto teaches of a first storage controller operable as a standalone storage controller (figs. 1, 7, 8, item 1-1-1; column 6, lines 56-60) comprising: a host interface configured for communicatively coupling a host computer system (figs. 1, 7, 8, item 50) to a first storage element (figs. 7, 8; item 11; column 7, lines 6 – 34; column 8, lines 1 – 17; where the channel IF unit connects the host computer to the hard disks via the SM and CM switches and the disk IF unit. Items 1-1-1 and corresponding item 5 comprise the first storage element);

a storage system interface configured for communicatively coupling the first storage element to a switching fabric (figs. 7, 8; column 7, lines 20 – 29; column 8, lines 1 – 17; where the disk array control unit (storage system interface) connects the hard drive to the SM and CM paths (switching fabric) through the disk IF unit and the SM and CM switches within);

a processor configured for processing I/O requests received through the storage system interface and the host interface to access physical storage locations (figs. 7, 8; item 101; column 9, lines 17 – 26, and 45 – 54; where the microprocessor receives a read data request from the host computer and determines which hard disk stores the requested data),

wherein the storage system interface is further configured for transferring a portion of the I/O requests through the switching fabric to a selected second storage controller (figs. 7, 8; column 9, lines 17 – 26, and 45 – 54; where the microprocessor determines which hard drive the requested data is stored on and sends the read request to the microprocessor in the disk IF unit corresponding to where the data is stored. for the part of the data located in a hard drive in the disk array control unit 1-1-2, the microprocessor in the channel IF unit in the disk array control unit 1-1-1 must transfer that request over the SM and CM paths (switching fabric) to the disk array control unit 1-1-2 (second storage controller))

Yoshida teaches of an interface for receiving an optional plug-in card (PIC) (fig. 6; column 12, lines 29-37; as the disk control units can be removed and added to the

disk control apparatus (PIC), they must include an interface that connects them together when they are added);

wherein the PIC provides additional circuitry to enable N-way connectivity between the first storage controller and any number of second storage controller to permit scaling of the first storage controller to operate in a network architecture storage system (fig. 4, 6; column 12, lines 22-50; where the disk control apparatus (PIC) contains a service processor, and various connection networks to connect the multiple disk control units)

15. With respect to claim 12, the combination of Fujimoto and Yoshida teaches of all the limitations of the parent claim as discussed supra. Fujimoto also teaches of wherein the first storage controller is adapted to route the portion of the I/O requests to the selected second storage controller (figs. 7, 8; column 9, lines 17 – 26, and 45 – 54; where the microprocessor determines which hard drive the requested data is stored on and sends the read request to the microprocessor in the disk IF unit corresponding to where the data is stored. For the part of the data located in a hard drive in the disk array control unit 1-1-2 (second storage controller), the microprocessor in the channel IF unit in the disk array control unit 1-1-1 (first storage controller) must transfer that request to the microprocessor in the disk IF unit located in the disk array control unit 1-1-2 (second storage controller)) and

wherein the portion of the requests are processed by the selected second storage controller for accessing physical storage locations coupled to the selected second storage controller (figs. 7, 8; column 9, lines 45 – 54; where the microprocessor

receiving the command in the disk IF unit of the disk array control unit 1-1-2 (second storage controller) reads the data out of the hard drive connected to it).

16. With respect to claim 16, Fujimoto teaches of a method of storing data, comprising: providing a first storage element having a first storage controller capable of interfacing with one or more host computer system and capable of operating as a stand alone storage controller in the first storage element (as previously cited),

at least one of:

transferring I/O requests from the host computer system to the first storage controller to access a plurality of physical storage locations within the first storage element (figs. 7, 8; column 9, lines 17 – 26, and 45 – 54; where the read out request is sent from the host computer to the disk array control unit 1-1-1. The microprocessor determines the location of the data requested and requests the microprocessor in the disk IF units of the corresponding hard drive to read out the data. If the data is located on a hard drive associated with the disk array control unit 1-1-1, then it is accessed by the microprocessor within the disk IF units of the disk array controller 1-1-1) and

Yoshida teaches of configuring the first storage controller to an add an optional plug-in card (PIC) to add capability of the first storage controller for N-way communication with any number of second storage controllers within any number of second storage elements (fig. 4, 6; column 12, lines 22-50; where the disk control units can be added or removed from the disk control apparatus (PIC) and the service processor manages the disk control units. The disk control apparatus (PIC) contains a

service processor, and various connection networks to connect the multiple disk control units);

The combination of Fujimoto and Yoshida teaches of transferring I/O requests from the host computer system via the PIC through the switching fabric to a selected second storage controller (Fujimoto; figs. 7, 8; column 9, lines 17 – 26, and 45 – 54; where the read out request is sent from the host computer to the disk array control unit 1-1-1 (first storage controller). The microprocessor determines the location of the data requested and requests the microprocessor in the disk IF units of the corresponding hard drive to read out the data. If the data is located in a hard drive connected to the disk array control unit 1-1-2 (second storage controller), the microprocessor in the channel IF unit in the disk unit 1-1-1 must transfer that read request over the SM and CM paths (switching fabric) to the disk array control unit 1-1-2. It is then received by the microprocessor within the disk IF units of the disk array controller 1-1-2 associated with the desired hard drive. The SM and CM paths are contained within the disk control apparatus (PIC) in the combination of Fujimoto and Yoshida).

17. With respect to claim 17, the combination of Fujimoto and Yoshida teaches of all the limitations of the parent claim as discussed supra. The combination of Fujimoto and Yoshida also teaches of wherein transferring I/O requests from the host computer system via the PIC through the switching fabric to the selected second storage controller comprises processing the I/O requests with the selected second storage controller to access physical storage locations within the second storage element (Fujimoto; figs. 7, 8; column 9, lines 17 – 26, and 45 – 54; where the read out request is

sent from the host computer to the disk array control unit 1-1-1 (first storage controller). The microprocessor determines the location of the data requested and requests the microprocessor in the disk IF units of the corresponding hard drive to read out the data. If the data is located in a hard drive connected to the disk array control unit 1-1-2 (second storage controller), the microprocessor in the channel IF unit in the disk unit 1-1-1 must transfer that read request over the SM and CM paths (switching fabric) to the disk array control unit 1-1-2. It is then received by the microprocessor within the disk IF units of the disk array controller 1-1-2 associated with the desired hard drive which reads out the data (processes the request). The SM and CM paths are located on the disk control apparatus (PIC) in the combination of Fujimoto and Yoshida).

18. Claims 3 – 5, 10, and 20 rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto and Yoshida as applied to claim 1, 6, and 16 respectively, and further in view of the applicant's prior art admission (AAPA).

19. With respect to claim 3, the combination of Fujimoto and Yoshida teaches of all the limitations of the parent claim as discussed supra. Fujimoto also teaches of wherein the switching fabric is an SAN switching fabric communicatively coupled to the first and the selected second storage controllers and configured for routing the I/O requests between the host computer system and the first and the second storage controllers (figs. 1, 8; column 8, lines 32 – 40; column 2, lines 31 – 47; where the SM and CM paths (SAN switching fabric) between the disk array control units are made up of SM and CM switches (121 and 122). A SAN is described in Fujimoto to be met by an

arrangement of a low level model of a conventional disk array controller connected to a plurality of identical controllers).

Fujimoto fails to explicitly teach of the SAN switching fabric comprising at least one of Fibre Channel and Infiniband. However, the applicant's admission of prior art teaches of the SAN switching fabric comprising at least one of Fibre Channel and Infiniband (spec. page 2, 2nd and 3rd paragraph).

The combination of Fujimoto and Yoshida, and the applicant's prior art admission are analogous arts as they are both in the same field of endeavor, storage systems and controllers. It would have been obvious to one of ordinary skill in the art to implement the Fibre Channel and/or Infiniband standards in the switching paths between the disk array controllers in Fujimoto. The motivation for this would have been to allow for a greater distance between the storage systems and the host systems (applicant's prior art admission, spec. page 2, 2nd paragraph).

20. With respect to claim 4, the combination of Fujimoto, Yoshida, and AAPA teach of all the limitations of the parent claims as discussed supra. The combination of Fujimoto, Yoshida, and AAPA also teaches of wherein the storage system is adaptable to identify physical storage locations of both the first and the second storage elements using the PIC added to the storage system when the first storage controller is adapted to communicate with the selected second storage controller (Fujimoto; figs. 7, 8, item 13; column 9, lines 20 – 27; where the microprocessors in any disk control unit can access the shared memory units in their and the other disk control units to determine the address and the hard disks that stores the requested data. In accessing between

the disk control units, the microprocessors use the disk control apparatus (PIC) in the combination to reach the other disk control unit).

21. With respect to claim 5, the combination of Fujimoto, Yoshida, and AAPA teach of all the limitations of the parent claims as discussed supra. The combination of Fujimoto, Yoshida, and AAPA also teaches of wherein the PIC when coupled to the first storage controller comprises an N-chip configured for communicatively coupling to the SAN switching fabric to route a portion of the I/O requests from the host computer system through the SAN switching fabric to the second storage controller (Fujimoto; figs. 7, 8, items 121, 122, column 8, lines 32 – 57; column 9, line 17-column 10, line 6; the SM and CM paths (SAN switching fabric) containing the SM and CM switches (N-chip) link the multiple disk control units allowing for requests to be sent between the disk control units. These SM and CM switches are embodied in the disk control apparatus (PIC) in the combination of Fujimoto, Yoshida, and AAPA),

wherein the N-chip is further configured for accessing data from the physical storage locations of both the first and the second storage elements (Fujimoto; figs. 7, 8, items 121, 122, column 8, lines 32 – 57; where the SM and CM switches in the paths are connected to the SM and CM switches in each disk control unit, enabling the accessing of the hard drives by the disk control units they are not directly connected to).

22. With respect to claim 10, the combination of Fujimoto and Yoshida teaches of all the limitations of the parent claim as discussed supra. The combination of Fujimoto and Yoshida also teaches of wherein transferring the first portion of the requests comprises switching the first portion of the requests via the PIC through a SAN switching fabric

(Fujimoto; figs. 7, 8; column 2, lines 31 – 47; column 9, lines 17 – 26, and 45 – 54; where the microprocessor in the channel IF unit of disk unit 1-1-1 determines which hard drive the requested data is stored on and sends the read request to the microprocessor in the disk IF unit corresponding to the hard drive that hold the data. For the part of the data located in a hard drive in the disk array control unit 1-1-2 (first portion of the requests), the microprocessor in the channel IF unit of disk unit 1-1-1 must transfer that request over the SM and CM paths (SAN switching fabric) between the units to the disk array control unit 1-1-2. A SAN is described in Fujimoto to be met by an arrangement of a low level model of a conventional disk array controller connected to a plurality of identical controllers. The SM and CM paths are located on the disk control apparatus (PIC) in the combination of Fujimoto and Yoshida).

The combination of Fujimoto and Yoshida fails to explicitly teach of a SAN switching fabric selected from at least one of Fibre Channel and Infiniband. However, the applicant's prior art admission teaches of a SAN switching fabric selected from at least one of Fibre Channel and Infiniband (spec. page 2, 2nd and 3rd paragraph).

23. With respect to claim 20, the combination of Fujimoto and Yoshida teaches of all the limitations of the parent claim as discussed supra. The combination of Fujimoto and Yoshida also teaches of wherein transferring the I/O requests comprises switching the I/O requests via the PIC through a SAN switching fabric (Fujimoto; figs. 7, 8; column 2, lines 31 – 47; column 9, lines 17 – 26, and 45 – 54; where the microprocessor in the channel IF unit of disk unit 1-1-1 determines which hard drive the requested data is stored on and sends the read request to the microprocessor in the disk IF unit

corresponding to the hard drive that hold the data. For the part of the data located in a hard drive in the disk array control unit 1-1-2, the microprocessor in the channel IF unit of disk unit 1-1-1 must transfer that request over the SM and CM paths (SAN switching fabric) to the disk array control unit 1-1-2. A SAN is described in Fujimoto to be met by an arrangement of a low level model of a conventional disk array controller connected to a plurality of identical controllers. The SM and CM paths are located on the disk control apparatus (PIC) in the combination of Fujimoto and Yoshida).

24. The combination of Fujimoto and Yoshida fails to explicitly teach of a SAN switching fabric selected from at least one of Fibre Channel and Infiniband. However, the applicant's prior art admission teaches of a SAN switching fabric selected from at least one of Fibre Channel and Infiniband (spec. page 2, 2nd and 3rd paragraph).

Response to Arguments

25. Applicant's arguments filed 1/31/2006 have been fully considered but they are not persuasive.

26. Applicant's arguments with respect to claims independent claims 1, 6, 11, and 16 have been considered but are moot in view of the new ground(s) of rejection.

27. The applicant alleges that Fujimoto does not show a first storage controller accessing storages devices of a second storage element nor the other way around. With reference to figure 8 and column 10, lines 7-22 of Fujimoto states that a host computer can access a hard drive by simply issuing an access request to the disk control unit the host computer is connected without regards to the location of the hard

drive. It also states that reading out of a hard drive connected to a different disk control unit than the one requested, the data is read out by way of the internal connections (CM and SM paths) instead of using the channel IF units of both disk control units; i.e. data is read from the hard drive via the disk IF unit to the cache memory (all in the same disk control unit, which is attached to the hard drive containing the data requested) to the requesting disk control unit (attached to the requesting host) via the CM and SM paths and to the host via the channel IF unit in the requesting disk control unit. Column 9, line 13 – column 10, line 6 exemplify this in more detail.

28. The examiner would also like to mention that In re Dulberg, 129 USPQ 348 shows that making an object removable has been rendered obvious.

Conclusion

29. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

30. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

32. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

33. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Krofcheck

MATTHEW D. ANDERSON
PRIMARY EXAMINER